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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,440	12/19/2001	Jae Young Park	K-0361	2090

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EXAMINER	
ROBERTS, BRIAN S	

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/021,440	PARK, JAE YOUNG	
	Examiner	Art Unit	
	Brian Roberts	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-8,10-13 and 18* is/are rejected.

7)☒ Claim(s) *9,14-17 and 19-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 have been examined.

Claim Objections

2. Claim 21 and 22 are objected to because of the following informalities:

- Claim 21 should read --The method of claim 19, further comprising assigning each of the plurality of STM interfaces experiencing a detectable fault *to* the standby state—
- Claim 22 depends from claim 21.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Katou. (US 5508997)

- In reference to claim 1-4

In Figure 1, the admitted prior art teaches:

- A UTOPIA interface that transmits UTOPIA level-2 data
- A pair of STM interfaces that receive UTOPIA level-1 data

- A UTOPIA FIFO memory that converts the UTOPIA level-2 data into the UTOPIA level-1 data and transfers the UTOPIA level-1 data to the pair of STM interfaces according to a transmission address

The admitted prior art does not teach a UTOPIA interface control part that converts the transmission address by inverting a value of a least significant bit in the transmission address, depending on assigned state, either standby or active, of the STM interfaces

In Figure 12A and12B, Katou teaches method of transmitting data to a system with an active unit and a standby unit. The active unit and standby unit each are assigned a different address. The state of each of the units changes in accordance with the conditions of the system. A source unit transmits data to the system containing the active and standby units. The source unit inherently contains a processor for determining the status (active or standby) of the units and a controller for attaching the destination address to the data according to the state of the devices. In the event that the active unit fails, the system switches from the active unit to the standby unit enabling processing to continue. Katou further teaches inverting the value of a least significant bit in the transmission address from "0B00" to "0B01" to change the destination address from an active to standby device. (column 1 lines 1-62)

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the system and method of the admitted prior art to include a active state STM-1 interface chip and a standby STM-1 interface chip and a controller (UTOPIA interface control part) to address the ATM cells to the proper STM-1 interface

chip according to the conditions of the system as taught by Katou because having an active unit and a standby unit makes it possible to perform processing continuously by switching over to the standby unit if the active unit fails. (column 1 lines 14-16)

- In reference to claim 10 and 12

In Figure 1, the admitted prior art teaches:

- A UTOPIA interface that transmits UTOPIA level-2 data
- A pair of STM interfaces that receive UTOPIA level-1 data
- A UTOPIA FIFO memory that converts the UTOPIA level-2 data into the UTOPIA level-1 data and transfers the UTOPIA level-1 data to the pair of STM interfaces according to a transmission address

The admitted prior art does not teach checking a fail state of the pair of STM interfaces, assigning one of the pair a standby state and another an active state, converting the transmission address by inverting a value of a least significant bit in the transmission address in accordance to the fail states of the pair of STM interfaces and transmitting the converted UTOPIA level-1 data to the STM interface having the active state, according to the transmission address.

In Figure 12A and12B, Katou teaches method of transmitting data to a system with an active unit and a standby unit. The active unit and standby unit each are assigned a different address. The state of each of the units changes in accordance with the conditions of the system. A source unit transmits data to the system containing the active and standby units. The source unit inherently contains a processor for

determining the status (active or standby) of the units and a controller for attaching the destination address to the data according to the state of the devices. In the event that the active unit fails, the system switches from the active unit to the standby unit enabling processing to continue. Katou further teaches inverting the value of a least significant bit in the transmission address from "0B00" to "0B01" to change the destination address from an active to standby device. (column 1 lines 1-62)

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the system and method of the admitted prior art to include the method of assigning a active interface and a standby interface and converting the transmission address by inverting a value of a least significant bit in the transmission address in accordance to the fail states of the pair of STM interfaces as suggested by Katou because having an active unit and a standby unit makes it possible to perform processing continuously by switching over to the standby unit if the active unit fails. (column 1 lines 14-16)

5. Claims 5,6,8,13 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Katou. (US 5508997), as applied to the parent claims, and further in view of Park. (US 6430197)

- In reference to claims 5,6,8,13 and 18

In Figure 1, the admitted prior art teaches:

- A UTOPIA interface that communicates UTOPIA level-2 data
- A pair of STM interfaces that communicate UTOPIA level-1 data

- A UTOPIA FIFO memory that converts the UTOPIA level-2 data into the UTOPIA level-1 data and transfers the UTOPIA level-1 data to the pair of STM interfaces, according to a transmission address
- A bus matching FIFO that converts the UTOPIA level-1 data from the STM interfaces into the UTOPIA level-2 data and transfers the converted UTOPIA level-2 data to the UTOPIA interface chip according to a reception address

The admitted prior art does not teach a processor for reading a pair of STM interfaces, a UTOPIA interface control part that converts the transmission address and reception address under the control of the processor.

In Figure 12A and12B, Katou teaches method of transmitting data to a system with an active unit and a standby unit. The active unit and standby unit each are assigned a different address. The state of each of the units changes in accordance with the conditions of the system. A source unit that transmits data to the system, inherently contains a processor for determining the status (active or standby) of the units and a controller for attaching the destination address to the data according to the state of the devices. Katou further teaches changing the source destination address and the destination address according to the status of the units. (column 1 lines 17-62)

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the system of the admitted prior art to include a active state STM-1 interface chip and a standby STM-1 interface chip and a controller (UTOPIA interface control part) to address the ATM cells to the proper STM-1 interface chip according to the conditions of the units of the system determined by a processor as

taught by Katou because having an active unit and a standby unit makes it possible to perform processing continuously by switching over to the standby unit if the active unit fails. (column 1 lines 14-16)

The combination of the admitted prior art and Katou teaches a system and method that covers substantially all limitations of the parent claim.

The combination of the admitted prior art and Katou does not teach each STM interface being connected to a separate bus-matching memory.

In Figure 3, Park teaches each physical layer device connected to a separate FIFO unit.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of the admitted prior art and Katou to include each STM-1 interface chip to be connected to a FIFO memory unit as suggested by Park because it allows the buffering and performing FIFO with respect to the ATM cells from each of the STM interfaces.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Katou. (US 5508997), as applied to the parent claims, and further in view of Park. (US 6430197) and further in view of Prasad et al. (US 6275491)

- In reference to claim 7

The combination of the admitted prior art, Katou, and Park teaches a system and method that covers substantially all limitations of the parent claim.

The combination of the admitted prior art, Katou, and Park does not explicitly teach a programmable logic device for reading the state of the pair of STM interfaces.

In Figure 5, Prasad et al. teaches a system utilizing a programmable logic device to perform logic control.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of the admitted prior art, Katou, and Park to include a programmable logic device as taught by Prasad et al. to determine the states of the pair of STM interfaces because the programmable logic device can perform control functions and can be readily reprogrammed to perform a different control function if the system changes.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Katou. (US 5508997), as applied to the parent claims, and further in view of Prasad et al. (US 6275491)

- In reference to claim 11

The combination of the admitted prior art and Katou teaches a system and method that covers substantially all limitations of the parent claim.

The combination of the admitted prior art and Katou does not explicitly teach a programmable logic device for reading the state of the pair of STM interfaces.

In Figure 5, Prasad et al. teaches a system utilizing a programmable logic device to perform logic control.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of the admitted prior art, Katou, and Park to include a programmable logic device as taught by Prasad et al. to determine the states of the pair of STM interfaces because the programmable logic device can perform control functions and can be readily reprogrammed to perform a different control function if the system changes.

Allowable Subject Matter

8. Claims 9, 14-17, and 19-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

- In reference to claims 9, 14-17, and 19-22

Claims 9, 14-17, and 19-20 are allowed because the prior record fails to teach or fairly suggest a synchronous transport module (STM) wherein the UTOPIA interface control part stores first bits, used to determine whether each of the pair of STM interfaces is assigned a duplex state or a simplex state, and second bits, used to determine whether each of the pair of STM interfaces assigned the duplex state is further assigned an active state or standby state.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure are:

- Kim et al. (US 5978377) teaches an STM-based ATM cell physical layer processing circuit.
- Jones et al. (US 6078595) teaches a timing synchronization and switchover from an active to standby unit in a network switch
- O'Neill et al. (US 6243382) teaches a method of interfacing to SAR devices in ATM switching apparatus.
- Yu (US 2001/0012288) teaches a data transmission apparatus and method for transmitting data between physical layer side device and network layer device.
- Lau et al. (US 6356561) teaches a method and apparatus for the fair and efficient transfer of variable length packets using fixed length segments.
- McWilliams (US 2002/0031132) teaches a UTOPIA-LVDS bridge.
- Smith et al. (US 6359858) teaches a switching redundancy control system and method.
- Hann et al. (US 6449655) teaches a method and apparatus for communication between network devices operating at different frequencies.
- Rich (US 6452927) teaches a method and apparatus for providing a serial interface between an ATM layer and a physical layer.
- Arato et al. (US 6535522) teaches a multiple protocol interface and method for use in a communication system.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Roberts whose telephone number is (571) 272-3095. The examiner can normally be reached on M-F 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BSR
10/11/2005

JOHN PEZZLO
PRIMARY EXAMINER